A Physics-Based GaAs PHEMT Noise Model for Low Drain Bias Operation Using Characteristic Potential Method

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***Abstract*—A new physics-based noise model of a GaAs PHEMT is developed using characteristic potential method" (CPM). The model calculates the intrinsic noise current sources using CPM. Combined with the extrinsic noise parameters extracted from the measured S-parameters, the model reproduces four noise parameters of the device accurately under low drain bias voltages without using any fitting parameters. The model is verified with a 0.2-μm GaAs PHEMT and shows excellent agreement with the measurements for all the noise parameters up to a drain voltage of 1 V. Also, the proposed method allows the simulation of the microscopic noise distribution and thus allows one to get physical understanding of noise mechanisms inside the device.**

***Index Terms*—Characteristic potential, Characteristic potential method, noise model, PHEMT.**

I. Introduction

THE noise model is required to understand the noise-generation mechanisms inside the device as well as to design low noise circuits. Numerous noise models have been proposed by a number of researchers [1]–[5]. Noise models for FETs reported so far can be classified into two categories, "physics-based model" (for example, Pucel [1], Gupta [2], and Pospieszalski [3] models) and "semi-empirical model" (Fukui [4] model). The former type is preferred in view of understanding and optimizing the noise performance of the devices. However, previously reported physics-based models require at least one fitting parameters that represent intrinsic noise contributions. These parameters need to be extracted from the noise parameter measurements. However, a complete noise measurement set up is complicated and costly, and it takes a long time for accurate calibration.

In this work, a physics-based GaAs PHEMT model that does not require any fitting parameters is developed using characteristic potential method (CPM). CPM was originally developed for mesoscopic devices in [6], and was extended to multi-terminal devices in [7]. Under low-voltage operation, the intrinsic device noise can be assumed to be dominated by the thermal noise, in which case the expressions for the intrinsic noise sources are exactly known. As will be shown later, CPM can be an effective method for calculating the intrinsic noise current density in this case. In this work, CPM was applied for FET noise modeling for the first time, and was used to develop a new physics-based noise model requiring no fitting parameters. The validity of the noise model is verified under low-voltage operation by comparison with the measured data.

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II. Noise Model Using CPM

Fig. 1 shows the noise equivalent circuit of a HEMT used in this work. It uses short circuit noise current sources (i_g, i_d) to model the intrinsic noise sources within a HEMT. To achieve a complete noise model, accurate information of the extrinsic elements is required as well as that of the intrinsic noise currents. Presented model uses "characteristic potential" to calculate the intrinsic noise currents, and uses measured S-parameters of the device to extract the extrinsic parameters.

The characteristic potential for the kth terminal (ϕ_k) of a given device is a function that is defined by a Laplace equation under a certain boundary conditions as follows:

$$\nabla \cdot [\sigma_s(\vec{r}) + j\omega\varepsilon(\vec{r})]\nabla\phi_k(\vec{r}, \omega) = 0 \qquad (1)$$

where the boundary conditions for ϕ_k are given by

$$\phi_k(\vec{r}, \omega)\,|_{A_m} = \delta_{k,m}, \quad \vec{n} \cdot \nabla\phi_k(\vec{r}, \omega)\,|_{A^*} = 0 \qquad (2)$$

where ϕ_k is the characteristic potential of electrode k, A_m is the contact area of electrode m, and A^* is the area except A_ms.

Under the assumption that thermal noise is the major noise mechanisms inside the device, which is a valid assumption at low drain voltages, the characteristic potentials can be used to calculate the power spectral density of the short circuit noise currents of the kth terminal $i_k(t)$, and the cross power spectral density of $i_k(t)$ and $i_m(t)$ using the following volume integrations [7]

$$\langle i_k^2 \rangle = 4KT \int_v dv \sigma_s(\vec{r})\nabla\phi_k(\vec{r}, \omega) \cdot \nabla\phi_k(\vec{r}, \omega)^* \Delta f \quad (3)$$

$$\langle i_k i_m^* \rangle = 4KT \int_v dv \sigma_s(\vec{r})\nabla\phi_k(\vec{r}, \omega) \cdot \nabla\phi_m(\vec{r}, \omega)^* \Delta f \quad (4)$$

Here, the position-dependent dc conductivity $(\sigma_s(\vec{r}))$ is found by a dc device simulator. Hot electron effect was not included in the simulation considering that our analysis is limited to low drain bias regions, where hot electron effects can be ignored. Our procedure for finding the intrinsic noise currents can be summarized as follows.

i) Obtain material properties such as position-dependent carrier concentrations, mobilities, and therefore conductivity (σ_s) inside the device from a device simulator by solving the Boltzmann transport equation. (Commercial dc simulator is used to carry out this step. Mobility model used in the simulation was field-dependent mobility model, and its parameters were optimized to improve the correspondence between measured and calculated I-V curve).

ii) Calculate the characteristic potentials for the gate and the drain terminals of the intrinsic FET by solving the corresponding Laplace equations (1) using an FEM simulator.

iii) Evaluate the noise current sources ($\langle i_g^2\rangle, \langle i_d^2\rangle$) and their correlation term by numerical integration (3)–(4).

Once the intrinsic noise sources and their correlation term are obtained, a noise equivalent circuit (Fig. 1) can be constituted with the knowledge of the FET equivalent circuit parameters. The equivalent circuit parameters were analytically extracted from the bias dependent S-parameters using a custom extraction program [8]. Intrinsic noise parameters can then be transformed to the chain noise representation using the correlation matrix method [9]. Finally, the four noise parameters of a two-port device are calculated by including the noise contributions from the extrinsic elements such as R_g, R_s, and R_d, using the well-known formulas [10].

In addition to the four noise parameters, the model allows one to probe inside the devices to find out the position-dependent noise contributions from each section of the FET. It is, therefore, very helpful in understanding physical noise mechanisms, and can be possibly extended to optimization of the device structures to minimize the noise.

III. Comparison With Measured Data

To verify the noise model, the four noise parameters predicted from the model are compared with the measured data at low drain biases from 2 to 23 GHz. The device used in the comparison is a 0.2-μm GaAs-based PHEMT.

The intrinsic noise sources of the HEMT and their correlation are plotted as a function of frequency in Fig. 2. As expected, S_{id} shows little frequency dependence while S_{ig} increases with frequency due to the enhanced capacitive coupling at high frequencies. Calculated noise parameters are compared with the measured data at two different drain biases (0.3 V: linear region and 1.0 V: slightly above knee voltage) in Figs. 3 and 4. Excellent agreement can be found at both bias voltages for all the noise parameters. Fit is slightly worse at 1 V, compared with that at 0.3 V, since the device is biased into the early saturation region and unaccounted noise sources may play nonnegligible roles.

The noise contribution inside the device has also been simulated, and the power density of drain noise current along the InGaAs channel is shown in Fig. 5. As expected, the highest noise contribution comes from the high-field region near the drain end of the gate electrode.

IV. Conclusion

A new physics-based noise model of GaAs PHEMT is developed using characteristic potential method. The model does not require any fitting parameters and show excellent agreement with the measured data for low drain bias voltages, where thermal noise is dominant. Since the model is capable of calculating the microscopic noise current at each portion of the device, it allows one to achieve physical understanding of noise mechanisms. The model can be further extended to higher drain bias voltages by including noise sources that have been ignored in the low-drain bias region. Our preliminary physical analysis shows that aside from the thermal noise, shot noise and hot electron noise can be major contributors to noise at higher drain biases. Upon the inclusion of these noise sources in the model, more practical physics-based models applicable to high drain bias region can be achieved.

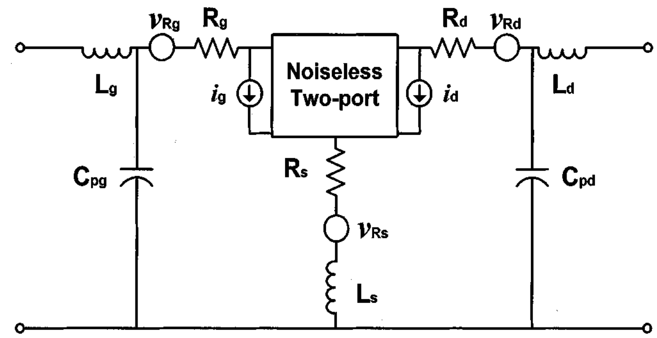

Fig. 1. FET noise equivalent circuit.

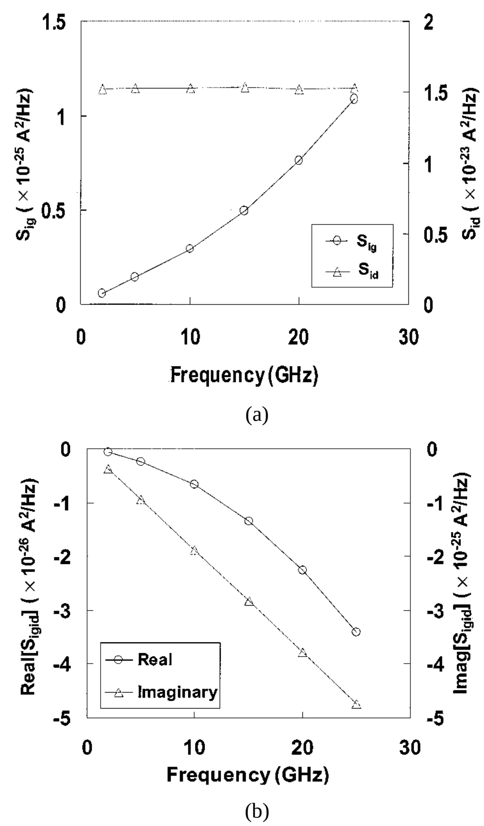

Fig. 2. (a) Calculated power spectral densities of the noise currents as a function of frequency. (b) Calculated cross power spectral density between noise currents as a function of frequency.

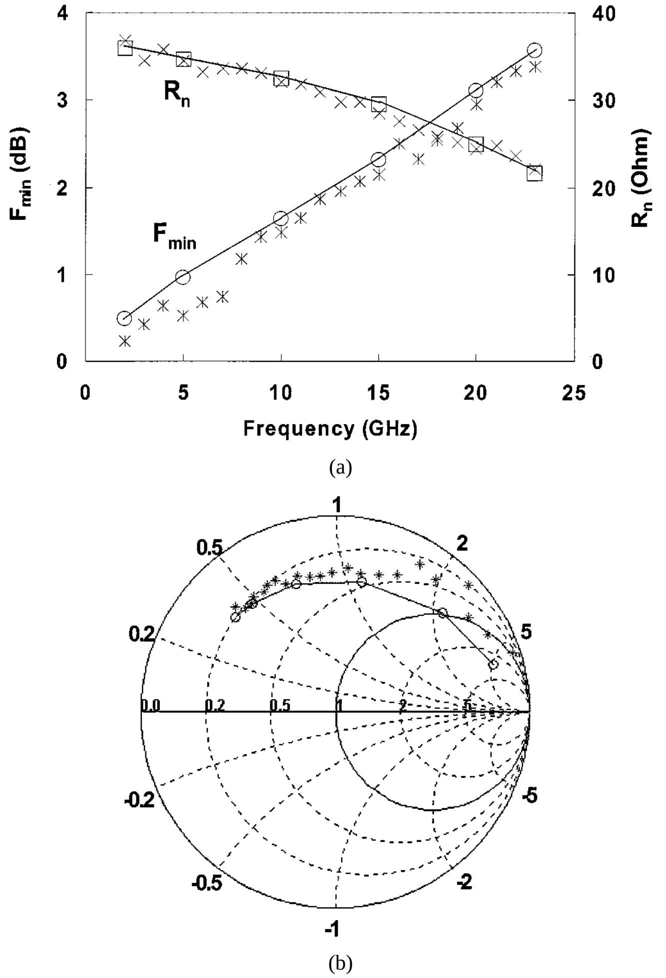

Fig. 3. Noise parameters at a low drain bias voltage ($V_g = -0.1$ V and $V_d = 0.3$ V) (⊖-,⊟-:calculated value, $*$, $\times$:measured value). (a) $F_{\min}$ and R_n; (b) $\Gamma_{\rm opt}$.

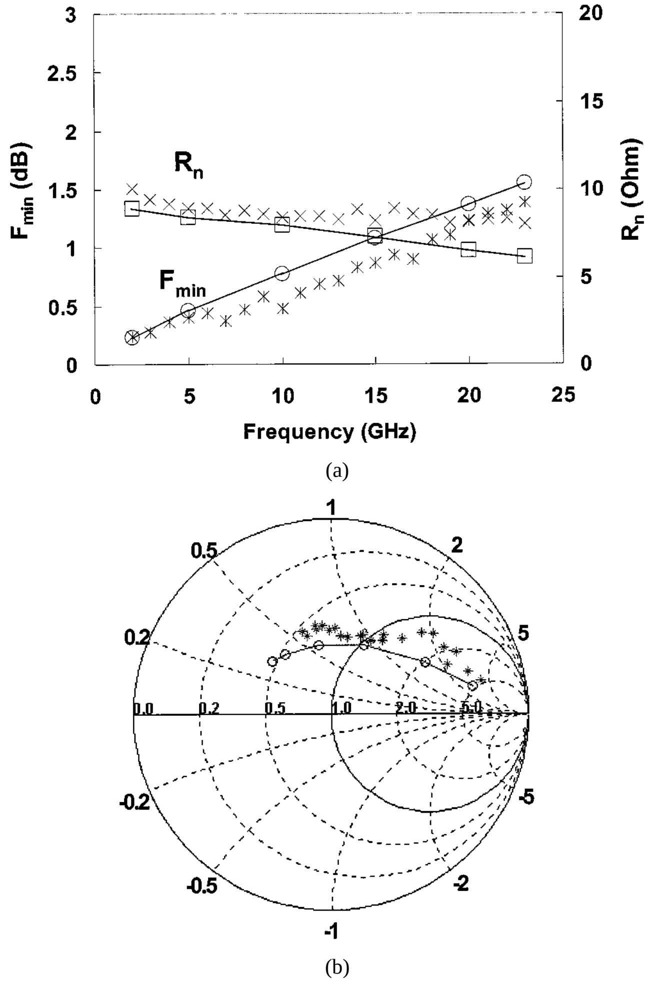

Fig. 4. Noise parameters at a higher drain bias voltage ($V_g = -0.2$ V and $V_d = 1$ V) (⊖-,⊟-:calculated value, $*$, $\times$:measured value). (a) $F_{\min}$ and R_n; (b) $\Gamma_{\rm opt}$.

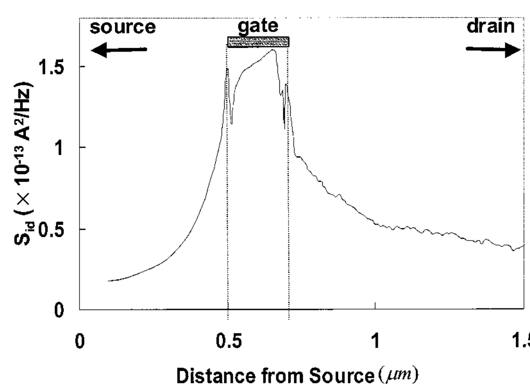

Fig. 5. Distribution of S_{id} along the InGaAs channel ($V_g = -0.1$ V, $V_d = 0.3$ V).

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